UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,912	02/27/2004	Kei-Wei Chen	67,200-1210	7509

7590 10/06/2005

TUNG & ASSOCIATES
Suite 120
838 W. Long Lake Road
Bloomfield Hills, MI 48302

EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,912	CHEN ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see pages 15 – 29, filed September 22, 2005, with respect to the rejection(s) of claim(s) 1 – 22 under 103 (a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art and explanations that follow.

Claim Objections

2. Claim 6 is objected to because of the following informalities: The word "comprises" inline 2 should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1, 2, 6, 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428.

Regarding claims 1 and 2, Chooi teaches a method for forming a copper dual damascene with improved copper migration resistance and improved electrical resistivity comprising the steps of:

- providing a semiconductor substrate 100 comprising upper 130 and lower 120 dielectric insulating layers separated by middle etch stop layer 125 (see Fig. 1e);
- forming a dual damascene opening by first forming a via 170 extending through a thickness of the upper and lower dielectric insulating layers (see Fig. 1e);
- then forming an upper trench line portion 150 extending through the upper dielectric insulating layer thickness and stopping at the middle etch stop layer 125 (see Fig. 1e and paragraph 9);

- blanket depositing a barrier layer 260 comprising at least one of a refractory metal and refractory metal nitride (see paragraph 50) to line the dual damascene opening (see Fig. 2e);
- removing a bottom portion of the barrier layer 260 to reveal an underlying conductive area 210 (see Fig. 2f); and,
- filling the dual damascene opening with copper to provide a substantially planar surface (see Fig. 2f) in paragraph 50.

Chooi fails to teach (1) etch stop layer comprising multiple layers and (2) forming an upper trench line portion extending through the upper dielectric insulating layer thickness and partially through the middle etch stop layer thickness including an uppermost layer comprising the middle etch stop layer.

Ngo teaches a middle etch stop layer 14 –16 (see Fig. 1) comprises at least two different material layers15 and 16 including a lowermost layer and an uppermost layer (element 1) and forming an upper trench line portion extending through the upper dielectric insulating layer thickness and partially through the middle etch stop layer thickness including an uppermost layer comprising the middle etch stop layer (element 2) with reference to Fig. 2 for the benefit of providing superior etch stopping capability and other properties as explained in column 6, lines 3 – 12.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi and provide the middle etch stop layer that comprises at least two different material layers including a lowermost layer and an

uppermost layer for the benefit of providing superior etch stopping capability and other properties as explained by Ngo in column 6, lines 3 – 12.

Regarding claim 6, Chooi teaches barrier layer of TiN, WN and TaN in paragraph 50.

Regarding claim 7, Chooi fails to teach n the barrier layer consists essentially of a Ta/TaN composite layer.

Ngo teaches barrier layer consisting essentially of a Ta/TaN composite layer in column 3, lines 36 – 39 for the benefit of fabricating semiconductor devices with high circuit speed in column 1, lines 6 – 10.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi and provide a Ta/TaN composite barrier layer for the benefit of fabricating semiconductor devices with high circuit speed as taught by Ngo in column 1, lines 6 – 10.

Regarding claim 8, Chooi teaches blanket deposition of barrier by a PVD process in paragraph 50.

Regarding claim 11, Chooi teaches underlying conductive area 110 of Cu in paragraphs 8 and 44.

Regarding claim 12, Chooi fails to teach the step of filling the dual damascene opening with copper comprises the steps of depositing a copper seed layer, carrying out an electro-chemical deposition process to fill the dual damascene opening with a copper filling and carrying out a CMP process to remove at least the copper filling portion overlying the dual damascene opening level.

Ngo teaches teach the step of filling the dual damascene opening with copper that comprises the steps of depositing a copper seed layer; carrying out an electro-chemical deposition process to fill the dual damascene opening with a copper filling; and, carrying out a CMP process to remove at least the copper filling portion overlying the dual damascene opening level in column 3, lines 39 – 45 for the benefit of fabricating semiconductor devices with high circuit speed in column 1, lines 6 – 10.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi and fill the dual damascene opening with copper that comprises the steps of depositing a copper seed layer; carrying out an electro-chemical deposition process to fill the dual damascene opening with a copper filling; and, carrying out a CMP process to remove at least the copper filling portion overlying the dual damascene opening level for the benefit of fabricating semiconductor devices with high circuit speed as taught by Ngo in column 1, lines 6 – 10.

7. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428 as applied to claim 1 above, and further in view of Kim, US 6,436,303.

Regarding claim 9, Chooi in view of Ngo fails to teach the step of removing the bottom portion of the barrier comprises a remote plasma etch treatment.

Kim teaches the remote plasma etch treatment for etching unwanted portion of a film deposited on a substrate with reference to Fig. 3 for the benefit of being less destructive to the substrate and less time consuming for etching unwanted portion of a film in column 1, lines 5 – 10.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi and employ a remote plasma etch process for the benefit of being less destructive to the substrate and less time consuming for etching unwanted portion of a film as taught by Kim in column 1, lines 5 – 10.

Regarding claim 10, Chooi in view of Ngo fails to teach wherein the remote plasma etch treatment comprises one of an RF and microwave power source.

Kim teaches the remote plasma etch treatment comprises one of an RF and microwave power source with reference to Fig. 1B for the benefit of being less destructive to the substrate and less time consuming for etching unwanted portion of a film in column 1, lines 5 – 10.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi and employ remote plasma etch treatment comprises one of an RF and microwave power source for the benefit of being less destructive to the substrate and less time consuming for etching unwanted portion of a film as taught by Kim in column 1, lines 5 – 10.

8. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428 as applied to claim 1 above, and further in view of Smith, US 6,642,141.

Chooi in view of Ngo fails to teach the middle etch stop layer comprises at least two different material layers selected from the group consisting of silicon nitride, silicon oxynitride, silicon carbide, and silicon oxycarbide.

Smith teaches middle etch stop layer that comprises at least two different material layers selected from the group consisting of silicon nitride and silicon oxynitride with reference to Fig. 1 in column 3, lines 43 – 60 for the benefit of better adhesion of the dielectric layers in column 2, lines 35 – 47.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi in view of Ngo and form the middle etch stop layer that comprises at least two different material layers selected from the group consisting of silicon nitride and silicon oxynitride for the benefit of better adhesion of the dielectric layers as taught by Smith in column 2, lines 35 – 47.

9. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428 as applied to claim 1 above, and further in view of Wu, US 2005/0110153.

Chooi in view of Ngo fails to teach the middle etch stop layer comprising a lowermost layer selected from the group consisting of silicon nitride and silicon oxynitride and an uppermost layer selected from the group consisting of silicon carbide, and silicon oxycarbide (claim 4) and the middle etch stop layer comprises a silicon oxynitride lowermost layer and a silicon carbide uppermost layer (claim 5).

Wu teaches middle etch stop layer comprising a lowermost layer selected from the group consisting of silicon nitride and silicon oxynitride and an uppermost layer selected from the group consisting of silicon carbide, and silicon oxycarbide and also the middle etch stop layer comprising a silicon oxynitride lowermost layer and a silicon

carbide uppermost layer in paragraphs 29 – 33 for the benefit of providing better etch selectivities to the different inter-metallic dielectric layers in paragraphs 2, 3 and 9.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Chooi in view of Ngo and form middle etch stop layer comprising a lowermost layer selected from the group consisting of silicon nitride and silicon oxynitride and an uppermost layer selected from the group consisting of silicon carbide, and silicon oxycarbide and also the middle etch stop layer comprising a silicon oxynitride lowermost layer and a silicon carbide uppermost for the benefit of providing better etch selectivities to the different inter-metallic dielectric layers as taught by Wu in paragraphs 2, 3 and 9.

10. Claims 13 and 16 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428 and Kim, US 6,436,303.

Limitations of these claims have been described earlier in rejecting claims 1, 2 and 6 – 12.

Regarding claim 19, Kim further teaches the remote plasma etch treatment comprises a remote plasma generator disposed upstream of an etch process chamber with reference to Fig. 3 for the benefit of being less destructive to the substrate and less time consuming for etching unwanted portion of a film in column 1, lines 5 – 10.

11. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi, US 2002/0064941 in view of Ngo, US 6,525,428 and Kim, US 6,436,303 as applied to claim 13 above, and further in view of Wu, US 2005/0110153.

Limitations of these claims have been described earlier in rejecting claims 4 and 5.

Double Patenting

12. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

13. Claims 1, 2, 6, 8, 11 and 12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 2 and 12 of U.S. Patent No. 6,878,615 in view of Ngo, US 6,525,428. Regarding claims 1, 2, 6, 8, 11 and 12, claims 1, 2 and 12 of US 6,878,615 teach forming the barrier layers only on the vertical walls of the trench as conforming to the Figs. 2a – 2i and most of the limitations.

However claims 1, 2 and 12 fail to teach etch stop layer comprising multiple layers and forming an upper trench line portion extending through the upper dielectric insulating layer thickness and partially through the middle etch stop layer thickness including an uppermost layer comprising the middle etch stop layer. However Ngo teaches this deficiency of Tsai, of US 6,878,615 as was explained earlier in rejecting

claims 1, 2, 6, 8, 11 and 12. Claim 6 corresponds to claim 10 of Tsai. Claim 11 corresponds to claim 12 of Tsai. Claim 12 corresponds to claim 1 of Tsai.

14. Claims 13,16 and 18 – 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 10 and 12 of U.S. Patent No. 6,878,615 in view of Ngo, US 6,525,428 and Kim, US 6,436,303.

Regarding claims 13, 16 and 18 – 22, claims 1, 2 and 12 of US 6,878,615 teach forming the barrier layers only on the vertical walls of the trench as conforming to the Figs. 2a – 2i.

However claims 1, 2 and 12 fail to teach etch stop layer comprising composite layers and forming an upper trench line portion extending through the upper dielectric insulating layer thickness and partially through the middle etch stop layer thickness and carrying out a remote plasma etch treatment to remove the bottom portion of the barrier layer to reveal the underlying conductive portion. However Ngo and Kim teach these deficiencis of Tsai, of US 6,878,615 as was explained earlier in rejecting claims 1 and 13. Claim 16 correspond to claim 10 of Tsai. Claim 21 corresponds to claim 12 of Tsai. Claim 22 corresponds to claim 1 of Tsai.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok K. Sarkar
October 3, 2005

Primary Examiner